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Whilham Curtis & Whilham
Reston International Center
11800 Sunrise Valley Dr
Suite 900
Reston, VA 20191

EXAMINER
GARBOWSKI, LEIGH M

ART UNIT	PAPER NUMBER
2825	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/678,742	Applicant(s) HUBAR ET AL.	
	Examiner Leigh Marie Garbowski	Art Unit 2825	

-- The MAILING DATE of this communication appears on the cover sheet with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 October 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *7-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 October 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

Claims 11, 19, 25 are objected to because of the following informalities: as per claims 11 and 25, "step" [line 2] should be --steps--; as per claim 19, "constrains" [line 1] should be –constraints–. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 14-15 and 17-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claims 14-15, there is no antecedent basis for "unused chip pads" [line 2] thus rendering the claims vague and indefinite.

As per claim 17, there is no antecedent basis for "a group of I/O cells" [lines 5-6], thus what is intended by the placing step [line 5] is not particularly clear. Also, there is no antecedent basis for "power rails and power return rails for at least two different power supplies" [lines 7-8], thus what is intended by the connecting step [line 7] is not particularly clear. Therefore, the claim is confusing, vague and indefinite.

As per claim 18, the language "to I/O cells to an I/O pad" is confusing, thus rendering the claim vague and indefinite.

The remaining claims, though not specifically mentioned, are rejected for incorporating the errors of their respective base claims by dependency.

Claim R jecti ns - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 7-8, 11-13, 18, 20-22 and 25-26 are rejected under 35 U.S.C. 102(a) as being anticipated by Zuchowski et al. ["I/O Impedance Matching Algorithm for High-Performance ASICs"].

Taking claims 7-8 and 11-12 as exemplary of the method as similarly recited, as per claim 7, Zuchowski et al. disclose a chip design method [figure 2] comprising: a) retrieving a wire width constraint from technology data for an I/O cell [page 2, first

column, lines 21-27]; b) retrieving a maximum resistance constraint from said technology data for said I/O cell [page 2, first column, lines 21-27]; c) propagating said wiring width constraint and said maximum resistance constraint to net design data for said chip [page 2, first column, lines 21-27]; d) generating said chip, connections between said I/O cell and an associated pad being constrained by said propagated constraints [pages 3-4, Chip Layout section]; and e) checking said IC [pages 3-4, Chip Layout section, Chip Checking and Release section]. As per claim 8, Zuchowski et al. further disclose wherein a plurality of I/O cells are wired [figure 2] and further comprising before the checking step (e), repeating steps (a) - (d) for each of said plurality of I/O cells [pages 3-4, Design Implementation section, Chip Layout section]. As per claim 11, Zuchowski et al. further disclose wherein the generating step (d) comprises: i) placing each of said I/O cells based on said propagated wire width and maximum resistance constraints; and ii) routing a connection between each said placed I/O cell and its associated pad, each said routed connection meeting said propagated wire width and maximum resistance constraints [page 2, first column, lines 21-27; pages 3-4, Design Implementation section, Chip Layout section]. As per claim 12, Zuchowski et al. further disclose wherein the checking step (e) comprises checking connections made in said generating step (d) against propagated wire width and maximum resistance constraints [page 2, first column, lines 21-27; pages 3-4, Chip Layout section, Chip Checking and Release section].

As per claim 13, Zuchowski et al. disclose a chip design method comprising: a) retrieving a power route pattern instruction [page 1, second column, lines 13-18; page 2,

first column, lines 21-27]; b) identifying power and power return connections [page 1, second column, lines 13-18; page 2, first column, lines 21-27]; c) routing each said power and each said power return connection, each said routed connection meeting wire width and maximum resistance constraints in said retrieved power route pattern instruction [pages 3-4, Chip Layout section]; and d) checking said wired IC [pages 3-4, Chip Layout section, Chip Checking and Release section].

As per claim 18, Zuchowski et al. disclose a system for IC chip design comprising: means for retrieving net constraints from technology data [page 2, first column, lines 21-27]; means for placing a plurality of I/O cells; and means for connecting each of said placed I/O cells to an I/O pad according to said retrieved net constraints [pages 3-4, Design Implementation section, Chip Layout section]. As per claim 20, Zuchowksi et al. further disclose: means for grouping I/O cells [figure 2]; and means for placing an ESD cell with each group of I/O cells [figure 2; pages 3-4, Design Implementation section, Chip Layout section].

Claims 13 and 18-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Blaauw et al. [U.S. Patent #5,689,432].

As per claim 13, Blaauw et al. disclose a chip design method comprising: a) retrieving a power route pattern instruction [column 2, lines 30-43]; b) identifying power and power return connections [column 2, line 41]; c) routing each said power and each said power return connection, each said routed connection meeting wire width and maximum resistance constraints in said retrieved power route pattern instruction [column 6, lines 10-20]; and d) checking said wired IC [figure 4].

As per claim 18, Blaauw et al. disclose a system for IC chip design [figures 2 and 4] comprising: means for retrieving net constraints from technology data [figure 1, element 10; column 2, lines 30-43]; means for placing a plurality of I/O cells [figure 1, element 12; column 6, lines 10-20]; and means for connecting each of said placed I/O cells to an I/O pad according to said retrieved net constraints [figure 1, elements 12-14; column 6, lines 10-20]. As per claim 19, Blaauw et al. further disclose wherein said retrieved constraints include power bussing constraints [column 2, line 41], further comprising: means for routing power and power return connections according to said power bussing constraints [figure 4, elements 28-32; column 6, lines 10-20].

Claims 7-8, 11-13, 18-19, 21-22, 25-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Ito [U.S. Patent #5,648,910].

Taking claims 7-8 and 11-12 as exemplary of the method as similarly recited, as per claim 7, Ito discloses a chip design method comprising: a) retrieving a wire width constraint from technology data for an I/O cell [column 4, lines 11-26]; b) retrieving a maximum resistance constraint from said technology data for said I/O cell [column 4, lines 11-26]; c) propagating said wiring width constraint and said maximum resistance constraint to net design data for said chip [column 4, line 60-column 5, line 7]; d) generating said chip, connections between said I/O cell and an associated pad being constrained by said propagated constraints [column 5, lines 43-51; column 6, line 62-column 7, line 25]; and e) checking said IC [column 3, lines 36-38]. As per claim 8, Ito further discloses wherein a plurality of I/O cells are wired [column 4, lines 48-49] and further comprising before the checking step (e), repeating steps (a) - (d) for each of said

plurality of I/O cells [column 7, lines 14-25]. As per claim 11, Ito further discloses wherein the generating step (d) comprises: i) placing each of said I/O cells based on said propagated wire width and maximum resistance constraints; and ii) routing a connection between each said placed I/O cell and its associated pad, each said routed connection meeting said propagated wire width and maximum resistance constraints [column 5, lines 43-51; column 6, line 62-column 7, line 25]. As per claim 12, Ito further discloses wherein the checking step (e) comprises checking connections made in said generating step (d) against propagated wire width and maximum resistance constraints [column 5, lines 43-51; column 6, line 62-column 7, line 25].

As per claim 13, Ito discloses a chip design method comprising: a) retrieving a power route pattern instruction [column 4, lines 11-26]; b) identifying power and power return connections [column 6, lines 30-33]; c) routing each said power and each said power return connection, each said routed connection meeting wire width and maximum resistance constraints in said retrieved power route pattern instruction [column 5, lines 43-51; column 6, line 62-column 7, line 25]; and d) checking said wired IC [column 3, lines 36-38].

As per claim 18, Ito discloses a system for IC chip design [] comprising: means for retrieving net constraints from technology data [column 4, lines 11-26]; means for placing a plurality of I/O cells [column 5, lines 43-51]; and means for connecting each of said placed I/O cells to an I/O pad according to said retrieved net constraints [column 5, lines 43-51; column 6, line 62-column 7, line 25]. As per claim 19, Ito further discloses wherein said retrieved constraints include power bussing constraints, further

comprising: means for routing power and power return connections according to said power bussing constraints [column 6, lines 30-33; 62-column 7, line 25].

Claims 7-8, 11-13, 18-22, 25-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Kang et al. [U.S. Patent #5,796,638].

Taking claims 7-8 and 11-12 as exemplary of the method as similarly recited, as per claim 7, Kang et al. disclose a chip design method comprising: a) retrieving a wire width constraint from technology data for an I/O cell [column 5, lines 20-37]; b) retrieving a maximum resistance constraint from said technology data for said I/O cell [column 5, lines 20-42]; c) propagating said wiring width constraint and said maximum resistance constraint to net design data for said chip [column 5, lines 42-47]; d) generating said chip, connections between said I/O cell and an associated pad being constrained by said propagated constraints [column 6, lines 20-35]; and e) checking said IC [column 4, lines 33-36]. As per claim 8, Kang et al. further disclose wherein a plurality of I/O cells are wired [column 6, lines 5-20] and further comprising before the checking step (e), repeating steps (a) - (d) for each of said plurality of I/O cells [column 6, lines 1-5]. As per claim 11, Kang et al. further disclose wherein the generating step (d) comprises: i) placing each of said I/O cells based on said propagated wire width and maximum resistance constraints; and ii) routing a connection between each said placed I/O cell and its associated pad, each said routed connection meeting said propagated wire width and maximum resistance constraints [column 5, lines 42-47; column 6, lines 6-35]. As per claim 12, Kang et al. further disclose wherein the checking step (e) comprises

checking connections made in said generating step (d) against propagated wire width and maximum resistance constraints [column 6, lines 1-5].

As per claim 13, Kang et al. disclose a chip design method comprising: a) retrieving a power route pattern instruction [column 5, lines 20-37]; b) identifying power and power return connections [column 7, lines 26-30]; c) routing each said power and each said power return connection, each said routed connection meeting wire width and maximum resistance constraints in said retrieved power route pattern instruction [column 5, lines 20-47; column 6, lines 21-35]; and d) checking said wired IC [column 4, lines 33-36].

As per claim 18, Kang et al. disclose a system for IC chip design [] comprising: means for retrieving net constraints from technology data [column 5, lines 20-37]; means for placing a plurality of I/O cells [column 6, lines 6-35]; and means for connecting each of said placed I/O cells to an I/O pad according to said retrieved net constraints [column 5, lines 20-47; column 6, lines 6-35]. As per claim 19, Kang et al. further disclose wherein said retrieved constraints include power bussing constraints, further comprising: means for routing power and power return connections according to said power bussing constraints [column 5, line 30; column 6, lines 21-35]. As per claim 20, Kang et al. further disclose: means for grouping I/O cells [column 6, lines 6-20]; and means for placing an ESD cell with each group of I/O cells [column 6, lines 21-35].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9, 14 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zuchowski et al. or Ito or Kang et al. or Blaauw et al. in view of Schweiss [U.S. Patent #5,155,065].

Zuchowski et al. or Ito or Kang et al. [as per claims 7-8, 13 and 21-22] or Blaauw et al. [as per claim 13] disclose the features from which the claim depends, however, neither teach wherein the routing step (c) includes identifying any unused chip pads and wiring said unused pad to a power rail or to a power return rail. Schweiss teaches a chip design method comprising routing I/O circuits and power connections, including wiring an unused pad [column 10, lines 37-40]. A person of ordinary skill in the art at the time of the invention would have found it obvious to combine these teachings because customer flexibility is increased.

Claims 10, 15 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zuchowski et al. or Ito or Kang et al. or Blaauw et al. in view of Sugasawara [U.S. Patent #6,043,539].

Zuchowski et al. or Ito or Kang et al. [as per claims 7-8, 13 and 21-22] or Blaauw et al. [as per claim 13] disclose the features from which the claim depends, however, neither teach wherein the routing step (c) includes identifying any unused chip pads and wiring said unused pad to a cell including an ESD protect device. Sugasawara teaches a chip design method comprising routing I/O circuits and power connections, including wiring an unused pad [column 2, lines 43-50]. A person of ordinary skill in the art at the

time of the invention would have found it obvious to combine these teachings because "improved ESD protection is provided ...without assign additional circuitry to the chip".

Allowable Subject Matter

Claim 16 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 17 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action.

The following is a statement of reasons for the indication of allowable subject matter: the prior art of record does not disclose or teach the methods as recited, particularly with respect to at least two different power supplies.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Masleid et al. [U.S. Patent #4,988,636] disclose grouping I/O circuits and ESD circuits. Amerasekera et al. [U.S. Patent #5,949,694] disclose optimizing an I/O circuit for ESD events. Braiman et al. disclose "Automated Generation of Custom Pad Cells for ASICs."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leigh Marie Garbowski whose telephone number is 703-305-9753. The examiner can normally be reached on days.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 703-308-1323. The fax phone numbers

for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-1782.

LEIGH M. GARBOWSKI
PATENT EXAMINER

Leigh Marie Garbowski
November 18, 2002